Orrick Docket No.: 703567.4001

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner	Panasonic Europe Ltd.		
Application No..	10/628,906	Filing Date	July 28, 2003
Entitled	Methods and Systems for Reducing Leakage in Semiconductor Circuits		
Name of Assignee	Panasonic Europe Ltd.		
Type of Assignee (corporation, partnership, university)	corporation		

states that it is:

1 ☒ the assignee of the entire right, title and interest; or

2 ☐ an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is _____%

in the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at
Reel_____, Frame_____, or a true copy of the original assignment is attached.

or

B. ☒ A chain of title from the inventors(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: Alan Marshall, et al. To: Elixent Limited
The document was recorded in the United Sates Patent and Trademark Office at
Reel 014960, Frame 0672, or for which a copy thereof is attached

2. From: Elixent Limited To: Panasonic Europe Ltd.
The document was recorded in the United Sates Patent and Trademark Office at
Reel 018471, Frame 0928, or for which a copy thereof is attached

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

☒ Copies of assignments or other documents in the chain of title are attached.

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee:

Signature	Daryl Daybell		
Date	November 10, 2006	Typed Name	Donald Daybell
Telephone	(949) 567-6700	Title	Attorney

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 1222 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comment on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NO SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patent, P.O. Box 1450, Alexandria, VA 22313-1450.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

AUGUST 09, 2004

PTAS

ORRICK, HERRINGTON & SUTCLIFFE LLP
DONALD DAYBELL
4 PARK PLACE, SUITE 1600
IRVINE, CA 92614-2558

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RECORDATION DATE: 02/09/2004

REEL/FRAME: 014960/0672
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BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).
DOCKET NUMBER: 703567.4001

ASSIGNOR:
MARSHALL, ALAN

DOC DATE: 01/27/2003

ASSIGNOR:
OLGIATI, ANDREA

DOC DATE: 01/28/2003

ASSIGNOR:
STANSFIELD, ANTHONY I.

DOC DATE: 01/27/2003

ASSIGNEE:
ELIXENT LIMITED
CASTLEMEAD, LOWER CASTLE STREET
BRISTOL BS1 3AG, UNITED KINGDOM

ORRICK IP PROSECUTION
Due Date 1.28.05
Action Item Status
Resp Atty DD
Docketed by CHW
Entered 8.13.04

SERIAL NUMBER: 10628906 FILING DATE: 07/28/2003
PATENT NUMBER: ISSUE DATE:
TITLE: METHODS AND SYSTEMS FOR REDUCING LEAKAGE CURRENT IN SEMICONDUCTOR CIRCUITS

DOROTHY WILLIAMS, PARALEGAL
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

02-11-2004

FORM PTO-1595
1-31-92

RECO

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

Docket No. 703567.4001

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof. 102667435

1. Name of conveying party(ies): 2-9-04
ALAN MARSHALL, ANDREA OLGIATI, AND ANTHONY I. STANSFIELD
Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party:
Name: ELIXENT LIMITED
Internal Address:
City: BRISTOL BS1 3AG Country: United Kingdom
Street Address: Castlemead, Lower Castle Street
City: BRISTOL BS1 3AG Country: United Kingdom
Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:
☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other
Execution Date: 1/27/03, 1/28/03

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is:
A. Patent Application No(s).: 10/628,906
B. Patent No(s).:
Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:
Name: **Donald Daybell**
Internal Address: Orrick, Herrington & Sutcliffe LLP
4 Park Place, Suite 1600
Irvine, CA 92614-2558
Customer No. 34313

6. Total number of applications and patents involved: one

7. Total fee (37 CFR 3.41): $ 40.00
☒ Enclosed.
☐ Charge this Deposit Account if any additional fee is required

8. Deposit Account Number: **15-0665**

DO NOT USE THIS SPACE

9. Statement and signature:

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Donald Daybell
Donald Daybell, Reg No. 50,877

Date: February 4, 2004

Total number of pages including cover sheet: 4

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02/11/2004 DBYRNE 00000013 10628906
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DOCSOC1:146990.1

CERTIFICATE OF MAILING
(37 C.F.R. §1.8a)

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

February 4, 2004
Date of Deposit

Sally Hartwell

Orrick Docket No.: 703567.4001

ASSIGNMENT OF PATENT APPLICATION

WHEREAS, WE, ALAN MARSHALL, a citizen of the UNITED KINGDOM, ANDREA OLGIATI, a citizen of ITALY, and ANTHONY I. STANSFIELD, a citizen of the UNITED KINGDOM, (hereinafter referred to as "ASSIGNORS"), have invented and own a certain invention entitled **METHODS AND SYSTEMS FOR REDUCING LEAKAGE CURRENT IN SEMICONDUCTOR CIRCUITS** for which application for Letters Patent of the United States of America has been assigned Serial No. 10/628,906; and

WHEREAS, **ELIXENT LIMITED** a corporation organized and existing under and by virtue of the laws of the United Kingdom and having its principal place of business at Castlemead, Lower Castle Street, Bristol BS1 3AG, United Kingdom (hereinafter referred to as "ASSIGNEE"), is desirous of acquiring the exclusive right, title and interest in, to and under said invention and in, to and under any Patent or similar legal protection to be obtained therefor in the United States of America, its territorial possessions and in any and all countries foreign thereto.

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, ASSIGNORS hereby sell, assign, transfer and set over unto the said ASSIGNEE, its successors and assigns, the full and exclusive right, title and interest to said invention and to all Letters Patent or application or similar legal protection, not only in the United States and its territorial possessions, but in all countries foreign thereto to be obtained for said invention by said application, and to any continuation, division, renewal, substitute or reissue thereof or any legal equivalent thereof in the United States or a foreign country for the full term or terms for which the same may be granted, including all priority rights under the International Convention; and ASSIGNORS hereby authorize and requests the United States Commissioner of Patents and Trademarks, and any officials of foreign countries whose duty it is to issue patents or any legal

equivalent thereof, to issue said patents to ASSIGNEE, its successors and assigns, in accordance with this Assignment

ASSIGNORS hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this Agreement;

ASSIGNORS further covenant with the said ASSIGNEE, its successors and assigns, that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said application, said invention and said Letters Patent and legal equivalents as may be known and accessible to ASSIGNORS and ASSIGNORS will testify as to the same in any interference or litigation related thereto and will promptly execute and deliver to ASSIGNEE or its legal representative any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents in the United States or in any foreign country, which may be necessary or desirable to carry out the purposes thereof. ASSIGNORS shall be entitled to reimbursement by ASSIGNEE for any reasonable expenses incurred in complying with the above covenant.

This document shall be governed by the laws of the United States of America and of the State of California.

WITNESS my hand at BILSTON, United Kingdom this 27th day of JAN, 2004

2004.

ALAN MARSHALL

WITNESS my hand at BRISTOL, United Kingdom this 28 day of January 2004.

ANDREA OLGIATI

WITNESS my hand at Bristol, United Kingdom this 27th day of January 2004.

ANTHONY I. STANSFIELD

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

NOVEMBER 03, 2006

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500174129A

DONALD DAYBELL
4 PARK PLAZA, SUITE 1600
IP PROSECUTION DEPARTMENT
IRVINE, CA 92614-2558

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RECORDATION DATE: 11/03/2006

REEL/FRAME: 018471/0928
NUMBER OF PAGES: 16

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).
DOCKET NUMBER: 703567.1

ASSIGNOR:
ELIXENT LIMITED

DOC DATE: 07/14/2006

ASSIGNEE:
PANASONIC EUROPE LTD.
3 FURSEGROUND WAY, STOCKLEY PARK
UXBRIDGE, MIDDLESEX, UNITED
KINGDOM
UB11 1DD

SERIAL NUMBER: 11006974
PATENT NUMBER:

FILING DATE: 12/07/2004
ISSUE DATE:

TITLE: METHODS AND SYSTEMS FOR REDUCING LEAKAGE CURRENT IN SEMICONDUCTOR CIRCUITS

SERIAL NUMBER: 10188388 FILING DATE: 07/01/2002
PATENT NUMBER: ISSUE DATE:
TITLE: LOOSELY-BIASED HETEROGENEOUS RECONFIGURABLE ARRAYS

SERIAL NUMBER: 11130613 FILING DATE: 05/16/2005
PATENT NUMBER: ISSUE DATE:
TITLE: LOOSELY-BIASED HETEROGENEOUS RECONFIGURABLE ARRAYS

SERIAL NUMBER: 09891736 FILING DATE: 06/25/2001
PATENT NUMBER: 6542394 ISSUE DATE: 04/01/2003
TITLE: FIELD PROGRAMMABLE PROCESSOR ARRAYS

SERIAL NUMBER: 09555624 FILING DATE: 06/01/2000
PATENT NUMBER: 6567834 ISSUE DATE: 05/20/2003
TITLE: IMPLEMENTATION OF MULTIPLIERS IN PROGRAMMABLE ARRAYS

SERIAL NUMBER: 10224093 FILING DATE: 08/19/2002
PATENT NUMBER: 6859084 ISSUE DATE: 02/22/2005
TITLE: LOW-POWER VOLTAGE MODULATION CIRCUIT FOR PASS DEVICES

SERIAL NUMBER: 10628906 FILING DATE: 07/28/2003
PATENT NUMBER: 6946903 ISSUE DATE: 09/20/2005
TITLE: METHODS AND SYSTEMS FOR REDUCING LEAKAGE CURRENT IN SEMICONDUCTOR CIRCUITS

ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

DATED 14 July 2006

ELIXENT LIMITED
(as "Assignor")

PANASONIC EUROPE LTD.
(as "Assignee")

DEED OF ASSIGNMENT OF INTELLECTUAL PROPERTY

McDERMOTT WILL & EMERY UK LLP
7 Bishopsgate
London
EC2N 3AR

Tel: 020 7577 6900
Fax: 020 7577 6950

TABLE OF CONTENTS

4B.

THIS DEED OF ASSIGNMENT OF INTELLECTUAL PROPERTY RIGHTS is made on the day of 14 July 2006

BETWEEN:

(1) **ELIXENT LIMITED**, (registered in England and Wales under number 04163347) whose registered office is at Temple Back East, Temple Quay, Bristol, BS1 6EG (the "**Assignor**"); and

(2) **PANASONIC EUROPE LTD.**, (registered in England and Wales under number 03329345) whose registered office is at 3 Furseground Way, Stockley Park, Uxbridge, Middlesex, UB11 1DD; (the "**Assignee**").

WHEREAS:

(A) The Assignor is the registered proprietor and/or the beneficial owner of and/or otherwise able to transfer its Intellectual Property, as defined below.

(B) This Deed has been entered into pursuant to an agreement to purchase the business of Elixent Limited of Temple Back East, Temple Quay, Bristol, BS1 6EG between the parties to this Agreement and Matsushita Electric Industrial Co., Ltd. (the "**Business Transfer Agreement**"), whereby the Assignor has agreed to transfer to the Assignee its Intellectual Property on the terms set out below.

IT IS AGREED THAT:

1. DEFINITIONS AND INTERPRETATION

1.1 In this Deed, unless the context requires otherwise the following expressions shall have the following meanings:

"**Business Transfer Agreement**" has the meaning set out in Recital (B);

"**Deed**" means this assignment;

"**Intellectual Property**" has the meaning ascribed to it in the Business Transfer Agreement, subject to the exclusion of any such Intellectual Property licensed to the Assignor;

"**Encumbrance**" has the meaning ascribed to it in the Business Transfer Agreement;

"**Patents**" means those patents detailed in schedule 1 hereto;

"**Trade Marks**" means those trade marks detailed in Schedule 2 hereto;

"**Warranties**" has the meaning ascribed to it in the Business Transfer Agreement.

1.2 The headings in this Deed are for convenience only and shall not affect the interpretation of this Deed.

1.3 Unless the context otherwise requires, references to clauses are to clauses of this Deed.

2. ASSIGNMENT

The Assignor hereby assigns to the Assignee all its rights, title and interest in the its Intellectual Property which includes, without limitation, the Trade Marks and the Patents and all goodwill associated therewith.

3. FURTHER ASSURANCE

The Assignor shall execute such further documents and do such further acts as the Assignee may reasonably request from time to time at the Assignee's expense by way of further assurance of the rights assigned pursuant to the provisions of this Deed.

4. WARRANTIES

No warranty is given regarding the Assignor's Intellectual Property except for the Warranties (insofar as they are applicable to the Assignor's Intellectual Property) which are given subject to the terms of the Business Transfer Agreement.

5. ENTIRE AGREEMENT

This Deed and the BTA sets out the entire agreement and understanding between the parties in respect of the subject matter of this Deed.

6. RIGHTS OF THIRD PARTIES

The Parties to this Deed do not intend that any of its terms will be enforceable by virtue of the Contracts (Rights of Third Parties) Act 1999 by any person not a party to it.

7. GOVERNING LAW

This Deed shall be governed by and construed in accordance with the law of England. Each party hereby irrevocably submits to the exclusive jurisdiction of the courts of England over any claim or matter arising under or in connection with this Deed.

AS WITNESS the wards of the Parties or their duly authorised representative on the day and year first before written.

SCHEDULE 1

Patents

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
1.	Field Programmable Processor Arrays (US) (Alan Marshall, Anthony Stansfield, Jean Vuillemin)	A rectangularly-arranged FPGA, wherein each row and each column contains alternating processing and switching sections.	US 6,252,792	Issued	June 26, 2001	July 13, 1999	January 29, 1997
2.	Field Programmable Processor Arrays (UK)	"	UK0956646 B1	Issued	April 2, 2003	January 28, 1998	January 29, 1997
3.	Field Programmable Processor Arrays (FR)	"	FR0956646 B1	Issued	April 2, 2003	January 28, 1998	January 29, 1997
4.	Field Programmable Processor Arrays (DE)	"	DE69812898 T2	Issued	April 2, 2003	January 28, 1998	January 29, 1997
5.	Field Programmable Processor Arrays (US)	Continuation of 6,252,792 – same disclosure, additional claims.	US 6,542,394	Issued	April 1, 2003	June 25, 2001	January 29, 1997
6.	Field Programmable Processor Arrays (JP)	Same disclosure, includes claims of 6,542,394 and additional claims.	H10-531759	Pending, awaiting exam.	-	January 28, 1998	January 29, 1997
7.	Field Programmable Processor Devices (US) (Alan Marshall, Anthony Stansfield, Jean Vuillemin)	An FPGA having switches for controlling an interconnect, and memory cells for storing data for controlling the switches, wherein isolating gates selectively isolate the memory from the interconnect.	US 6,262,908	Issued	July 17, 2001	July 13, 1999	January 29, 1997
#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date

8.	Field Programmable Processor Devices (UK)	"	UK0956645 B1	Issued	March 31, 2004	January 28, 1998	January 29, 1997
9.	Field Programmable Processor Devices (FR)	"	FR0956645 B1	Issued	March 31, 2004	January 28, 1998	January 29, 1997
10.	Field Programmable Processor Devices (DE)	"	DE69822796 T2	Issued	March 31, 2004	January 28, 1998	January 29, 1997
11.	Field Programmable Processor Devices (JP)	"	H10-531755	Pending, awaiting exam.	-	January 28, 1998	January 29, 1997
12.	Reconfigurable Processor Devices (US) (Alan Marshall, Anthony Stansfield, Jean Vuillemin)	A programmable array containing ALUs in which the function of an ALU is determined by the output of another ALU.	US 6,353,841	Issued	March 5, 2002	December 11, 1998	December 17, 1997
13.	Reconfigurable Processor Devices (UK)	"	UK0924625 B1	Issued	November 17, 2004	November 24, 1998	December 17, 1997
14.	Reconfigurable Processor Devices (FR)	"	FR0924625 B1	Issued	November 17, 2004	November 24, 1998	December 17, 1997
15.	Reconfigurable Processor Devices (DE)	"	DE69827589 T2	Issued	November 17, 2004	November 24, 1998	December 17, 1997
16.	Reconfigurable Processor Devices (US)	Continuation of 6,353,841 – Same disclosure, additional claims.	US 6,553,395	Issued	April 22, 2003	November 28, 2001	December 17, 1997
17.	Reconfigurable Processor Devices (JP)	Same disclosure, includes claims of US continuation.	H10-359745	Pending, awaiting exam.	-	December 17, 1998	December 17, 1997

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
18.	Method and Apparatus	A circuit for combining an	US 6,523,107	Issued	February	December	December 17,

	for Providing Instruction Streams to a Processing Device (US) (Anthony Stansfield, Alan Marshall, Jean Vuillemin)	external instruction stream and an internally-stored instruction value and routing portions of the combined instruction to different parts of a processing device.			18, 2003	11, 1998	1997
19.	Method and Apparatus for Providing Instruction Streams to a Processing Device (Europe)	"	EP0924602 A2	Pending, awaiting exam.	-	November 24, 1998	December 17, 1997
20.	Method and Apparatus for Varying Instruction Streams Provided to a Processing Device Using Masks (US)	Continuation of 6,523,107 – Same disclosure, additional claims.	US 6,820,188	Issued	November 16, 2004	January 6, 2003	December 17, 1997
21.	Method and Device for Providing Instruction Streams to a Processing Device (JP)	Same disclosure, includes claims of US continuation.	H10-357686	Issued	January 20, 2006	December 16, 1998	December 17, 1997

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
22.	Implementation of Multipliers in Programmable Arrays (US) (Alan Marshall, Anthony Stansfield, Jean Vuillemin)	Creation of multiplier circuits in a programmable array, such that the function of an ALU in the multiplier is dynamically programmable based on the incoming bits being multiplied, thereby reducing the number of components in the multiplier.	US 6,567,834	Issued	May 20, 2003	June 1, 2000	December 17, 1997
23.	Implementation of Multipliers in Programmable Arrays (UK)	"	UK 1038216 B1	EP-Issued, UK Validation in progress	June 14, 2006	December 16, 1998	December 17, 1997
24.	Implementation of Multipliers in Programmable Arrays (FR)	"	FR1038216 B1	EP-Issued, FR Validation in progress	June 14, 2006	December 16, 1998	December 17, 1997
25.	Implementation of Multipliers in Programmable Arrays (DE)	"	DE registration number pending (EP1038216 B1)	EP-Issued, DE Validation in progress	June 14, 2006	December 16, 1998	December 17, 1997

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
26.	Implementation of Multipliers in Programmable Arrays (JP)	"	2000-539405	Pending, awaiting exam.	-	December 16, 1998	December 17, 1997
27.	Low-Power Voltage Modulation Circuit for Pass Devices (US) (Anthony Stansfield, Alan Marshall)	Modulated power supply voltages are provided to transistors within a logic device, so that degraded input voltages supplied to the transistors are sufficient to turn the transistors on or off, thereby avoiding leakage current.	US 6,859,084	Issued	February 22, 2005	August 19, 2002	August 19, 2002
28.	Low-Power Voltage Modulation Circuit for Pass Devices (EP)	"	EP1537666 A2	Pending, response to office action filed.	-	August 1, 2003	August 19, 2002
29.	Low-Power Voltage Modulation Circuit for Pass Devices (JP)	"	2004-530071	Pending, awaiting exam.	-	August 1, 2003	August 19, 2002
30.	Methods and Systems for Reducing Leakage Current in Semiconductor Circuits (US) (Alan Marshall, Andrea Olgiati, Anthony Stansfield)	An FPGA with low-threshold pass devices, wherein the pass devices are placed in a state that prevents leakage current across them. Claims directed to reconfigurable devices.	US 6,946,903	Issued	September 20, 2005	July 28, 2003	July 28, 2003

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
31.	Methods and Systems for Reducing Leakage Current in Semiconductor Circuits (EP)	Same disclosure, includes selected claims as filed in 6,946,903, to reconfigurable devices and circuits.	EP1519487 A1	Pending, awaiting exam	-	July 28, 2004	July 28, 2003
32.	Methods and Systems for Reducing Leakage Current in Semiconductor Circuits (JP)	Same disclosure, includes selected claims as filed in 6,946,903, to reconfigurable devices and circuits.	2004-220840	Pending, awaiting exam.	-	July 28, 2004	July 28, 2003
33.	Methods and Systems for Reducing Leakage Current in Semiconductor Circuits (US)	Divisional of 6,946,903 – Same disclosure, includes circuit claims filed in 6,946,903 and restricted out, as well as additional circuit claims.	11/006,974	Pending, response to office action filed.	-	December 7, 2004	July 28, 2003
34.	Loosely Biased Heterogeneous Reconfigurable Arrays (US) (Anthony Stansfield)	A heterogeneous array includes clusters of processing elements. The clusters include a combination of ALUs and multiplexers linked by direct connections and various generalpurpose routing networks. The multiplexers are controlled by the ALUs in the same cluster, or alternatively by ALUs in other clusters, via a dedicated multiplexer control network.	10/188,388	Pending, awaiting exam.	-	July 1, 2002	July 1, 2002

#	Title/Inventors	Brief Description	Registration/ Serial No	Status	Issue Date	Application Date	Earliest Claimed Priority Date
35.	Loosely Biased Heterogeneous Reconfigurable Arrays (EP)	"	EP1535394 A2	Pending, response to office action filed.	-	June 2, 2003	July 1, 2002
36.	Loosely Biased Heterogeneous Reconfigurable Arrays (JP)	"	2004-516568	Pending, awaiting exam.	-	June 2, 2003	July 1, 2002
37.	Loosely Biased Heterogeneous Reconfigurable Arrays (US) (Nicholas Ray, Andrea Olgiati, Anthony Stansfield, Alan Marshall)	Continuation-in-part of 10/188,388. Includes additional disclosure and claims directed to an array with a general-purpose network and a specialized multiplexer select network.	11/130,613	Pending, awaiting exam.	-	May 16, 2005	July 1, 2002 (CIP of 10/188,388)
38.	Loosely Biased Heterogeneous Reconfigurable Arrays (PCT)	PCT counterpart to 11/130,613	Awaiting receipt of serial number from WIPO	Pending awaiting exam.	-	May 16, 2006	May 16, 2005

PCT/EP2006/004604
Dec8
11/2/2006

SCHEDULE 2

Trademarks

Trade mark	Application/ Registration no	Classes	Country	Current Status
ELIXENT	1092706	9, 42	Canada	Registered
ELIXENT	200204436	9	Hong Kong	Registered
ELIXENT	200204437	42	Hong Kong	Registered
ELIXENT	751987	9, 42	International including Singapore, China (class 45 only), Japan (word and Japanese characters), France, Germany, Italy, Spain, Sweden, Finland, Benelux and Switzerland	Registered
ELIXENT	2001/99729	9, 42	Japan	Registered
ELIXENT	905002	9	Taiwan	Registered
ELIXENT	905001	42	Taiwan	Registered
ELIXENT	2242857	9, 42	UK	Registered
ELIXENT	76/212120	9	USA	Registered
ELIXENT	76/976728	35, 42	USA	Registered. Awaiting corrected Certificate of Registration.
ELIXENT	990460	9	India	Application was advertised on 1 November 2005.
D – Fabrix	2003 – 44107	9, 42	Japan	Registered
D – Fabrix	78/309832	9, 42	USA	Declaration of use filed 1 December 2005.

EXECUTED as a DEED
by ELIXENT LIMITED

DIRECTOR

~~**SECRETARY**~~

DIRECTOR
VLH.

Executed as a Deed)
by **Panasonic Europe Ltd.**)
acting by:)

HITOSHI OTSUKI

Chief Executive Officer and Director

MASATOSHI OHIRA)

Chief Financial Officer and Director

Signature of witness:

Name: Katsuhiko Ueda

Address: 1 Kotari-yakemachi Nagaokakyo City, Kyoto 617-8520 Japan